MONOLITHIC CIRCUITS FOR 60 GHz COMMUNICATION SYSTEMS USING PSEUDOMORPHIC HEMT PROCESS

P. Gamand, P. Suchet, M. Iost, M. Pertus, A. Collet, J. Bellaiche
Laboratoires d'Electronique Philips / Philips Microwave Limeil
22, avenue Descartes, 94453 Limeil-Brévannes Cedex, France
Phone 33.1.45.69.96.10 - Fax 33.1.45.69.44.77

P.A. Rolland, N. Haeze
Université de Lille - Département Hyperfréquences et Semiconducteurs
59655 Villeneuve d'Ascq Cedex, France
Phone 33.1.20.43.44.01 - Fax 33.1.20.43.25.53

Abstract

A wide band image rejection mixer and a high real estate efficiency amplifier have been designed and fabricated with a 0.25 μm pseudomorphic HEMT process. The mixer itself integrated on 0.6 mm^2, includes an in-phase power splitter, two single ended mixers and a quadrature phase shifter. It exhibits better than 30 dB of image rejection from 52 to 60 GHz RF band with 14 dB of conversion loss including the power splitter. Combined with two 0.3 mm^2 IF monolithic amplifiers, the mixer exhibits 8 to 9 dB of conversion gain from 0.5 to 3 GHz IF frequency bandwidth. The amplifier, operating around 62-63 GHz, exhibits better than 8 dB/mm^2 gain density, with an I/O VSWR of 2.5.

Introduction

The development of MMIC's in the millimeter wave domain is driven both by advances in technology and by the growth of the applications in military/professional and civil areas. At this level, the active device is no more the unique key factor to make mm-wave IC's competitive compared with hybrid technology. The capability to design compact circuits, combined of course with a calibrated technological process allows to win the challenge.

Circuit design

Non linear modelling has been done on PHEMT's from typical wafers in order to design the mixer. An image rejection mixer has first been designed. The RF signal is applied at the source of the transistor while the LO signal is injected through the gate. Matching networks have been synthesized to match the ports of the mixer. The IF frequency band covers the 0.1 to 5 GHz frequency bandwidth. The lowest IF frequency is limited by the RC time constant where R is the output resistance of the mixer at IF port and C the input capacitance of the load (i.e. the IF amplifier). The predicted conversion loss was 10 dB at 58 GHz. To split the RF signal in-phase, a Wilkinson splitter using lumped elements has been used. Its simulated insertion loss was 4 to 4.5 dB in the 52 to 60 GHz band. A Lange coupler has been designed to ensure a 0 to 90° phase shift between the two LO driving signals.

Figure 1 presents the simulated spectrum of the different signals across the mixer, the IF port being loaded by a high impedance. To provide gain conversion, two small size IF MESFET amplifiers have been used.

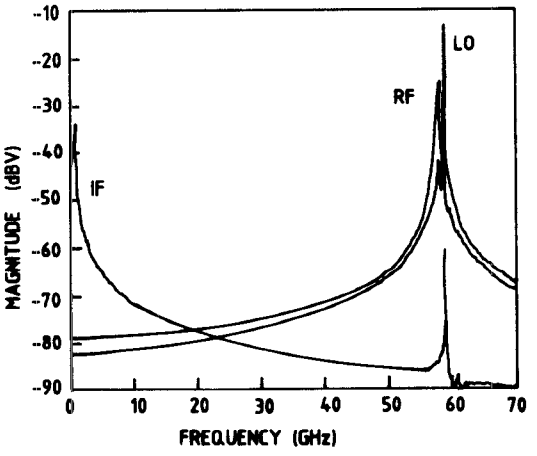

Figure 1
Simulated spectrum of the RF, LO and IF signals

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The amplifier has been designed using LC and lossy matching design techniques. In order to increase the real estate efficiency above 60 GHz, open stubs, quarter wavelength transmission lines have been eliminated in the gain stages (resistive feedback networks have also been used to avoid stability problems). The objective was to reach 8 to 10 dB/mm^2 gain density at 63 GHz.

Circuit fabrication and results

The circuits have been fabricated on a calibrated GaInAs/GaAs heterostructure grown by MOCVD. The gate is defined by e-beam lithography and the process includes conventional steps for vias, capacitors and air bridges. The MMIC's have been mounted in a ridge wave guide package using microstrip lines on teflon substrate.

Figure 2 presents a microphotograph of the image rejection mixer. The chip size is 0.6 mm^2. The conversion loss is 14 dB from 52 to 60 GHz for a fixed LO at 60 GHz. The RF and LO SWR's are respectively better than 2.5 and 1.7 over the band. The image rejection level is better than 30 dB over the 0.1 to 5 GHz IF frequency band. By adding monolithic IF amplifiers in the package, 8 to 9 dB of conversion gain is obtained.

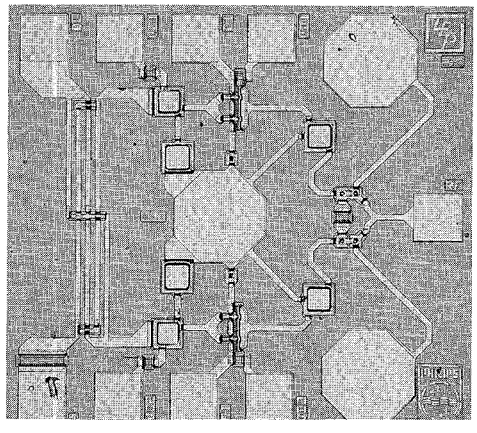

Figure 2
Microphotograph of the image rejection mixer

Figure 3 presents the evolution of the conversion gain and the rejection of the mixer with its IF amplifiers under two bias conditions:
Curve A is obtained by tuning the Vgs of the transistors each 500 MHz while curve B is obtained with fixed bias voltages. In any case, the rejection is close to 30 dB.

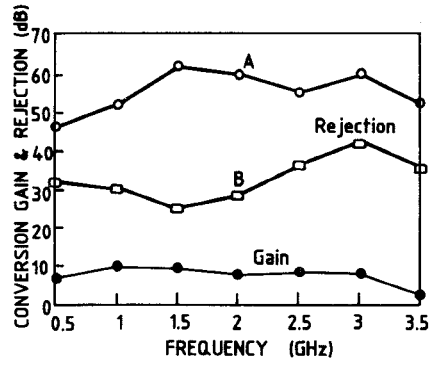

Figure 3
Evolution of the conversion gain and of the rejection level of the mixer

Figure 4 presents the microphotograph of the amplifier. The chip size is 0.9 mm^2 and the measured results show a real estate efficiency of 8 dB/mm^2 which is close to the objective and is state of the art [1], [2]. The input SWR can be derived from ***Figure 5***. It is less than 2.5 in the 60 to 64 GHz band. The output power at 1 dB gain compression 0 dBm across the bandwidth.

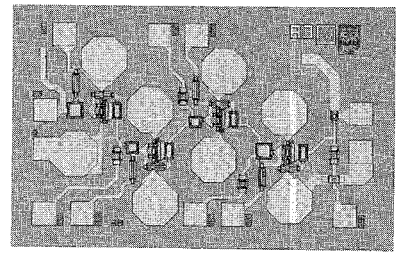

Figure 4
Microphotograph of the amplifier

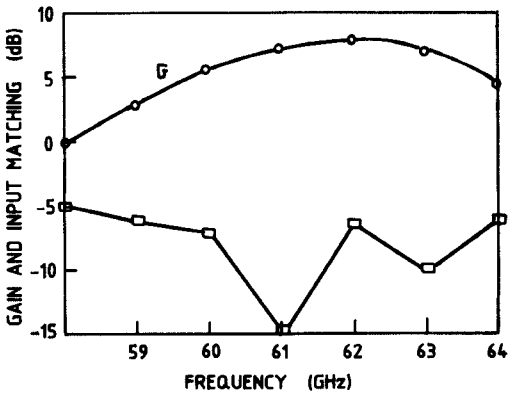

Figure 5
Performance of the amplifier
(V_{ds} = 4 V, V_{gs} = - 0.2 V)

Conclusion

Monolithic IC's operating around 60 GHz have been designed and fabricated. In particular, an image rejection mixer with only 0.6 mm^2 of chip area and with better than 30 dB of rejection from 52 to 60 GHz has been demonstrated and 8 dB/mm^2 of gain density has been obtained at 62 GHz. These circuits have been fabricated using a 0.25 μm PHEMT technology. This technology and the maturity of the design techniques show the feasibility of monolithic integration of complex circuits in millimeter wave domain.

Acknowledgements

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